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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/897,953	07/24/1997	HIDEHIKO KIRA	950107A	5157

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	08/897,953	KIRA ET AL.	
	Examiner	Art Unit	
	David E. Graybill	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5,6,8-10 and 15-18* is/are pending in the application.

4a) Of the above claim(s) *9 and 10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5,6,8 and 15-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10-31-7 has been entered.

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 5, 6, 8, 15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art, Maeda (English translation, JP58-180091), and Koga (JP4302444).

In the instant specification, at page 1, line 23 to page 2, line 22, applicant admits as prior art the following:

Re claim 15: A fabrication method of a semiconductor device comprising the steps of: (a) forming a plurality of projection electrodes 14 on each of a plurality of semiconductor chips 11; (b) applying a thermosetting insulating adhesive 18 to areas of mounting parts where the semiconductor chips are to be mounted on a substrate 17; (d) aligning the semiconductor chips to the mounting parts of the substrate at a first stage; (e) performing a first fixing of the semiconductor chips by pressing the semiconductor chips with a first pressure by a "bonding head" to which the semiconductor chips are absorbed, the semiconductor chips each being pressed separately (e.g. as illustrated in FIGS. 1E); and (g) heating the substrate, on which the semiconductor chips are fixed, with a thermosetting temperature of the thermosetting insulating adhesive.

Re claim 5: The fabrication method of the semiconductor device as claimed in claim 15, wherein said plurality of the projection electrodes are formed as studs by wire-bonding, the studs being leveled.

Re claim 6: The fabrication method of the semiconductor device as claimed in claim 15, wherein said step (a) further comprises the steps of (a-1) forming a conductive adhesive on said projection electrodes.

Re claim 8: The fabrication method of the semiconductor device as claimed in claim 6, wherein in the step (a-1), said conductive adhesive on the projection electrodes is formed by a conductive adhesive, that has been skidded on a plate, and then transcribed onto the projection electrodes.

Re claim 18: A method for mounting a plurality of semiconductor chips onto a substrate, comprising: forming a plurality of projection electrodes on each of the semiconductor chips; applying a thermosetting insulating adhesive to areas of the substrate where the semiconductor chips are to be mounted; aligning the semiconductor chips to the substrate; pressing the semiconductor chips aligned onto the substrate by a head with a first pressure by pressing only; and heating the semiconductor chips in a thermosetting temperature of the thermosetting insulating adhesive.

To further clarify, applicant's admitted prior art discloses a plurality of semiconductor chips because applicant discloses "FIGS. 1A to 1E show illustrations for explaining fabrication procedures of ***a conventional flip-***

chip-type semiconductor device [emphasis added]," and, "a semiconductor chip." Furthermore, "it is well settled that the term 'a' or 'an' ordinarily means 'one or more'." Tate Access Floors, Inc., and Tate Access Floors Leasing, Inc., v. Interface Architectural Resources, Inc., 279 F.3d 1357; 2002 U.S. App. LEXIS 1924; 61 U.S.P.Q.2D (BNA) 1647 ((citing Tate Access Floors, Inc. v. Maxcess Techs., Inc, 222 F.3d 958, 966 n.4, 55 U.S.P.Q.2D (BNA) 1513, 1518 [**32] (citing Elkay Mfg. Co. v. Ebco Mfg. Co., 192 F.3d 973, 977, 52 U.S.P.Q.2D (BNA) 1109, 1112 (Fed. Cir. 1999): "As we have previously explained, it is generally accepted in patent parlance that 'a' or 'an' can mean 'one or more'.")). And, "This court has repeatedly emphasized that an indefinite article 'a' or 'an' in patent parlance carries the meaning of 'one or more' in open-ended claims containing the transitional phrase 'comprising.' Unless the claim is specific as to the number of elements, the article 'a' receives a singular interpretation only in rare circumstances when the patentee evinces a clear intent to so limit the article." (Citations omitted). Scanner Technologies v./COS Vision Systems, 365 F.3d 1299, 1304 (Fed. Cir. 2004).

To further clarify, applicant's admitted prior art discloses pressing the semiconductor chips aligned onto the substrate by a head with a first pressure by pressing only because the adverbial phrase "by pressing only" modifies the word "pressing" and the pressing is by pressing only.

Furthermore, as reasoned from well established legal precedent, it would have been obvious to eliminate any heating during the pressing if it is not desired. Ex parte Wu, 10 USPQ 2031 (Bd. Pat. App. & Inter. 1989). In re Larson, 340 F.2d 965, 144 USPQ 347 (CCPA 1965). In re Kuhle, 526 F.2d 553, 188 USPQ 7 (CCPA 1975). MPEP 2144.04IIA.

However, applicant does not appear to explicitly admit as prior art a plurality of chips and the following:

Re claim 15: (c) heating the thermosetting insulating adhesive on the substrate with a half-thermosetting temperature so as to harden the thermosetting insulating adhesive to a half-thermosetting state by heating means; (f) moving the substrate to a second stage, while the semiconductor chips on the mounting parts of the substrate are held at their position by the half-thermosetting state of the thermosetting insulating adhesive; and (g) thereafter heating, at the second stage, the substrate, on which the semiconductor chips are fixed, with a thermosetting temperature of the thermosetting insulating adhesive.

Re claim 18: heating the thermosetting insulating adhesive on the substrate by heating means with a half-thermosetting temperature to half-harden the thermosetting insulating adhesive.

Nonetheless, at page 2, lines 19-20; page 3, line 22 to page 5, line 3; page 6, antepenultimate paragraph to page 8, line 3; and page 9, first full

paragraph, Maeda discloses heating "first heating process" a thermosetting insulating adhesive 3 on the substrate 1 with a half-thermosetting temperature so as to harden the thermosetting insulating adhesive to a half-thermosetting state "increase viscosity" by heating means 4; moving the substrate to a second stage, while the semiconductor chips on the mounting parts of the substrate are held at their position by the half-thermosetting state of the thermosetting insulating adhesive; and thereafter heating "second heating process", at the second stage, the substrate, on which the semiconductor chips are fixed, with a thermosetting temperature of the thermosetting insulating adhesive, and performing a second fixing of the semiconductor chips.

Moreover, it would have been obvious to combine the process of Maeda with the process of applicant's admitted prior art because it would enable accurate alignment of plural chips before the final fixing step of the conventional art.

Further, the combination of applicant's admitted prior art and Maeda does not appear to explicitly disclose the following:

Re claim 15: performing the second fixing with a second pressure, the plurality of semiconductor chips being pressed simultaneously in the second fixing.

Re claim 18: pressing the semiconductor chips with a second pressure while heating the semiconductor chips by a heating block.

Nevertheless, in the English abstract and figures, Koga discloses performing a second fixing with a second pressure, a plurality of semiconductor chips 1 being pressed simultaneously in the second fixing and pressing the semiconductor chips with a second pressure while heating the semiconductor chips by a heating block 25. Furthermore, it would have been obvious to combine the process of Koga with the process of the applied prior art because it would facilitate bonding.

Also, the combination of applied prior art does not appear to explicitly disclose the following:

Re claim 15: wherein the second pressure for performing the second fixing of the semiconductor chips is greater than the first pressure for performing the first fixing of the semiconductor chips.

Moreover, it would have been obvious to try the particular claimed relative pressures because "a person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense." KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385 (U.S. 2007). See also, Pfizer Inc. v. Apotex Inc., 82 USPQ2d 1852 (Fed. Cir. 2007). Moreover, as reasoned from well established

legal precedent, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed relative pressure limitations because applicant has not disclosed that, in view of the applied prior art, the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another pressure. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.'" In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969), Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(III), "Applicant can rebut a

prima facie case of obviousness based on overlapping ranges by showing the criticality of the claimed range. 'The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range.' In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP § 716.02 - § 716.02(g) for a discussion of criticality and unexpected results."

Also, the applied prior art does not appear to explicitly disclose the following:

Re claim 15: so that a dispersion of a degree of collapse of the plurality of projection electrodes may be absorbed.

Nonetheless, this limitation is merely a statement of intended use of the process that does not appear to result in a manipulative difference between the claimed process and the process of the applied prior art.

Furthermore, because the process of the applied prior art appears to be inherently capable of being used for the same intended use, the statement of intended use does not patentably distinguish the claimed process from the process of the applied prior art. Indeed, in the specification, at page 10, lines 4-6, applicant discloses that the mere

practice of the claimed process wherein the second pressure is set larger than the first pressure enables the intended use of the process.

Claims 5, 6, 8, 15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art, Maeda and Koga as applied to claims 5, 6, 8, 15 and 18 supra, and further in combination with Sakata (JP4-62946).

Applicant's admitted prior art, Maeda and Koga do not appear to explicitly disclose a process wherein the second pressure is greater than the first pressure.

Notwithstanding, in the English abstract, partial translation, and figures, Sakata disclosees this process. Furthermore, it would have been obvious to combine the process of Sakata with the applied prior art because it would enhance production yield.

To further clarify, Sakata disclosees that the first pressure is 20 kg/cm^2 and the second pressure is about 20 kg/cm^2, and the range encompassed by the phrase "about 20 kg/cm^2" encompasses a pressure greater than the first pressure of 20 kg/cm^2.

Indeed, this rejection was upheld in the affirmance of the examiner's answer elucidated in the Decision On Appeal filed on 7-19-5:

> However, we are in complete agreement with the examiner that the claimed subject matter would have been obvious to one of ordinary skill in the art within the meaning of § 103 in view of the applied prior art. Accordingly, we will sustain the examiner's rejections for essentially those reasons expressed

in the Answer, and we add the following primarily for emphasis. There is apparently no dispute that the admitted prior art found in appellants' specification is directed to a method of fabricating a semiconductor device by using a thermosetting insulating adhesive to mount a plurality of semiconductor chips on a substrate. The admitted prior art discussed in the specification does not include first heating the adhesive with a half-thermosetting temperature and applying a first pressure, and then, at a second stage, heating with the thermosetting temperature of the adhesive while applying a second pressure. However, we concur with the examiner that Maeda and Sakata evidence the obviousness of utilizing two heating stages for a bonding adhesive in making electrical devices, and Koga and Sakata support the obviousness of employing a second pressure to permanently affix the bonded components. Maeda teaches that the initial heating increases the viscosity of the adhesive to prevent the components from shifting before application of the final heating temperature. Also, Sakata teaches bringing the adhesive to a semi-hardened state and testing the operation of the device before applying the final hardening temperature. As for the specific temperatures and pressures to be used at the first and second stages, we totally agree with the examiner that it would be a matter of obviousness for one of ordinary skill in the art to resort to routine experimentation to determine the optimum temperatures and pressures. We simply find no merit in appellants' contention that the "claimed relation between the first and second pressure would require undue experimentation to produce" (page 15 of Brief, second paragraph).

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art, Maeda and Koga, as applied to claims 5, 6, 8, 15 and 18, and further in combination with DiStefano (5548091).

Applicant's admitted prior art, Maeda and Koga do not appear to explicitly disclose the following:

Re claim 16: A fabricating method according to claim 15, wherein in the heating step (c), heating the thermosetting insulating adhesive is performed by a heat plate on which the substrate is placed.

Nonetheless, at column 9, lines 3-63, DiStefano disclosees a process comprising wherein in a heating step, heating an adhesive is performed by a

heat plate 58 on which a substrate mounting chips is placed. In addition, it would have been obvious to combine the process of DiStefano with the process of the applied prior art because, both processes are directed to the same purpose of heating an adhesive, and it would facilitate adhesive curing.

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art, Maeda, Koga and Sakata, as applied to claims 5, 6, 8, 15 and 18, and further in combination with DiStefano (5548091).

DiStefano is applied for the same reasons it is applied supra.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art, Maeda and Koga as applied to claims 3, 5, 6, 8 and 15, and further in combination with Fujimoto (55480915115545).

Applicant's admitted prior art, Maeda and Koga do not appear to explicitly disclose the following:

Re claim 17: A fabrication method according to claim 15, wherein in the heating step (e), heating the thermosetting insulating adhesive is performed by a heat block having a plurality of pressing/heating heads each of which is provided on the heat block corresponding to the mounting parts of the substrate.

Notwithstanding, as cited, Koga disclosees a process comprising a heat block 25 having a plurality of pressing/heating portions each of which is provided on the heat block corresponding to the mounting parts of the substrate. Further, at column 6, line 52 to column 7, line 3, Fujimoto disclosees a single bonding head 52 for each chip. Moreover, it would have been obvious to combine the process of Fujimoto and the process of Koga by providing the heat block 25 with a single head for each chip because it would enable a pressing force to act evenly on each chip. Furthermore, it would have been obvious to combine the heat block of Fujimoto and Koga with the applied prior art because it would facilitate bonding.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art, Maeda, Koga and Sakata as applied to claims 5, 6, 8, 15 and 18, and further in combination with Fujimoto (5115545).

Fujimoto is applied for the same reasons it is applied supra.

Applicant's amendment and remarks filed 10-31-7 have been fully considered and are adequately treated supra and elsewhere in the record.

In addition, applicant argues that the applied prior art does not disclose various elements which were addressed by the Board of Patent Appeals and Interferences in the Decision On Appeal filed on 7-19-5 thusly:

> However, we are in complete agreement with the examiner that the claimed subject matter would have been obvious to one of ordinary skill in the art

within the meaning of § 103 in view of the applied prior art. Accordingly, we will sustain the examiner's rejections.

For information on the status of this application applicant should check PAIR: Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (571) 273-8300.

David E. Graybill
Primary Examiner
Art Unit 2822

D.G.
17-Jan-08